VERIFICATION OF TRANSLATION

I, the undersigned, declare that I am fluent in the English and Korean languages. I am competent to translate the attached document in Korean into English, and the above English translation of the document is accurate and complete.

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[Abstract of Disclosure]

[Abstract]

Semiconductor devices with a salicide layer and methods for fabricating the same are provided. The device comprises a field insulation layer formed in a substrate to define an active region, a gate pattern formed on the active region, and source/drain regions formed in active region at both sides of the gate pattern. Sidewall spacers are formed on sidewalls of the gate pattern, and a blocking insulation layer is formed on the isolation layer and on a portion of the active region neighboring the isolation layer. A silicide layer is formed on the source/drain regions between the blocking insulation layer and the sidewall spacers. The method comprises forming an isolation layer in a semiconductor substrate to define an active region, forming a gate pattern on the active region, implanting impurities into the active region at both sides of the gate pattern, and forming a spacer insulation layer on an entire surface of the semiconductor substrate with the gate pattern. The spacer insulation layer has a region becoming thinner from the isolation layer to the gate pattern.

[Representative Figure]

Fig. 3

[Specification]

[Title of the Invention]

SEMICONDUCTOR DEVICE HAVING SILICIDE LAYERS AND METHOD OF FABRICATING THE SAME

[Brief Description of the Drawings]

Figs. 1 and 2 are cross-sectional views showing a conventional method for fabricating semiconductor devices.

Figs. 3 through 5 are cross-sectional views showing a method for fabricating semiconductor devices according to a first exemplary embodiment of the present invention.

Figs. 6 through 11 are cross-sectional views showing a method for fabricating semiconductor devices according to a second exemplary embodiment of the present invention.

[Detailed Description of the Invention]

[Object of the Invention]

[Field of the Invention and Prior Art related to the Invention]

The present invention generally relates to methods of fabricating semiconductor devices and more specifically to methods of fabricating silicide layers aligned to source/drain regions.

As one of methods for fabricating semiconductor devices, there has been proposed a method for forming a silicide layer on source/drain regions and on a polysilicon gate. The silicide layer has various available

advantages such as providing good ohmic contact, lowering resistance of the polysilicon gate, a role as an etch stop layer to the source/drain region and the polysilicon gate. A conventional process for forming a silicide layer is a self-aligned silicide process, which is a salicide process. The salicide process includes a step of forming a metal layer, for instance, formed of cobalt, nickel or titanium combining silicon without reacting with a silicon oxide layer and a silicon nitride layer. The metals react with silicon to form a low-resistance silicide such as $CoSi_2$, NiSi or $TiSi_2$. The salicide process is applied to the semiconductor substrate with a gate electrode and source/drain region to form an aligned silicide layer on the source/drain regions and on the gate electrode with exposed silicon. The salicide process may form a thin and uniform silicide layer on the source/drain region and on the gate electrode.

A trench isolation layer is used for electrically isolating unit element to each other in processes for fabricating semiconductor devices. However, the trench filed isolation layer has a disadvantage that a dent is formed on a boundary with the active region.

Figs. 1 and 2 are cross-section views showing a conventional method for fabricating semiconductor devices.

Referring to Fig. 1, an isolation layer 12 is formed in a semiconductor substrate 10 to define an active region 14 by a trench isolation technique. As widely known, a dent may be formed in the isolation layer 12 neighboring the active region 14.

Referring to Fig. 2, a gate pattern 16 is formed on the active region 14, and source/drain regions 18 are formed in the active region neighboring

the gate electrode 16. Sidewall spacers 20 are formed on sidewalls of the gate electrode 16. Continuously, a conventional salicide process is applied to the resultant structure to form a silicide layer 22 on the source/drain regions 18 and the gate pattern 16. If there is a dent on a boundary between the active region 14 and the isolation layer 12, the silicide layer 22 is formed along a topology of the dent because the silicide layer provided by the salicide process is thin and uniform. Therefore, the silicide layer 22 may form a deep spike 26 to a bottom of the substrate in the dent D. As a result, leakage current occurs due to a focusing of electrical field through the spike 26 in a recent shallow source/drain structure for preventing a short channel effect and a punch through.

[Object of the Invention]

An object of the present invention is to provide semiconductor device without a silicide layer on a dent of isolation layer and methods of fabricating the same.

Another object of the present invention is to provide a semiconductor device for preventing leakage current due to a structure of the silicide layer and a method of fabricating the same.

Still another object of the present invention is to provide a method of fabricating a semiconductor device with thin source/drain regions with a silicide layer and a method of fabricating the same.

[Construction of the Invention]

In some embodiments, there is provided a semiconductor device

with a blocking insulating layer formed on the active region neighboring an isolation layer for preventing a formation of silicide layer. The device comprises a field insulation layer formed in a substrate to define an active region, a gate pattern formed on the active region, and source/drain regions formed in active region at both sides of the gate pattern. Sidewall spacers are formed on sidewalls of the gate pattern, and a blocking insulation layer is formed on the isolation layer and on a portion of the active region neighboring the isolation layer. A silicide layer is formed on the source/drain regions between the blocking insulation layer and the sidewall spacers. The silicide layer has a boundary aligned to edges of the blocking insulation layer and the sidewall spacers. The sidewall spacer may comprise, for example, an L-shaped inner spacer and an outer spacer. The inner spacer is formed on the sidewall of the gate pattern and on the active region neighboring the gate pattern, and the outer spacer having curved sidewall is formed on the inner space.

The isolation layer may include a dent at the region neighboring the active region. The blocking insulation layer is formed on the dent, such that the silicide layer does not formed thereon.

In some embodiments, there is provided a method for fabricating semiconductor devices for preventing a formation of silicide layer by forming a blocking insulation layer on an active region neighboring an isolation layer. The method comprises the following steps. First, an isolation layer is formed in a semiconductor substrate to define an active region. Then, a gate pattern is formed on the active region, and impurities are implanted into the active region at both sides of the gate pattern. A spacer

insulation layer is formed on an entire surface of the semiconductor substrate with the gate pattern. The spacer insulation layer has a region becoming thinner from the isolation layer to the gate pattern. In any of the embodiments, the spacer insulation layer is deposited in an ambient of chamber having long mean free path, thereby being formed to have thin thickness around the bottom edges of the gate pattern.

The spacer insulation layer is anisotropically etched to form sidewall spacers on sidewalls of the gate pattern, and to leave a blocking insulation layer on the isolation layer and on a portion of the active region neighboring the isolation layer. A silicidation process is applied to the semiconductor substrate to form a silicide layer on the source/drain regions between the blocking insulation layer and the sidewall spacers. Since the silicide layer is not formed on the blocking insulation layer, the silicide layer has a boundary aligned to the edges of the blocking insulation layer and the sidewall spacer.

In any of the embodiments, the spacer insulation layer is etched by high plasma power, as raising up an etch rate of the region neighboring the gate pattern, such that the sidewall spacers are formed and the blocking insulation layer is on the active region neighboring the isolation layer.

The present invention will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of

the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present.

Figs. 3 through 5 are cross-sectional views showing a method for fabricating a semiconductor device according to one embodiment of the present invention.

Referring to Fig. 3, an isolation layer 52 is formed in a semiconductor substrate 50 to define an active region 54. The isolation layer 52 may be formed by a conventional shallow trench isolation (STI) technique. When a trench isolation layer is formed by the STI technique, a dent D may be formed adjacent to the active region 54. There has been proposed various techniques for forming an isolation layer but it is still probable to be formed a dent due to a wet etching or a wet cleaning process after a isolation process.

A gate pattern 56 is formed on the active region 54. The gate pattern 56 crosses over the active region 54 and the isolation layer 52 (not shown). A spacer insulation layer 60 is formed on a semiconductor substrate 50 with the gate pattern 56. The spacer insulation layer 60 may be formed of silicon oxide or silicon nitride.

The spacer insulation layer 60 is formed thin at the region neighboring the gate pattern 56 and becomes thick from the gate pattern 56 to the isolation layer 52. In case of forming a material layer, the spacer insulation layer 60 is thickest around upper edges of the gate pattern 56

and thinnest around lower edges of the gate pattern 56 as improving deposition characteristics such as 3D effect or shadowing effect. That is to say, the spacer insulation layer 60 is formed thinnest at the active region 54 neighboring the gate pattern 56.

The shadow effect increases under the condition of long mean free path of reaction gas and low surface migration. Therefore, the spacer insulation layer 60 may be formed effectively at an ambient of chamber having low temperature and low pressure. Preferably, the spacer insulation layer 60 may be formed of low temperature oxide (LTO) or low temperature nitride (LTN) that is formed by LPCVD.

Referring to Fig. 4, the spacer insulation layer 60 is etched using an anisotropic plasma etching method to form sidewall spacers 60s on sidewalls of the gate pattern 56. In this case, the thin spacer insulation layer 60 on the active region neighboring the gate pattern 56 is entirely removed, the thick spacer insulation layer 60 on the active region neighboring the isolation layer 52 is left to form a blocking insulation layer 60a for covering the dent D. The region neighboring the gate pattern 56 is etched rapidly, such that the spacer insulation layer 60 neighboring the gate pattern 56 may be removed without exposing the dent D. Generally, the etch rate can be raised at the region neighboring the pattern by increasing bias power of the chamber.

Referring to Fig. 5, a silicide layer 62 is formed on the active region 54 exposed between the spacer insulation layer 60 and the blocking insulation layer 60a by applying a silicidation process to the semiconductor substrate 50. When the gate pattern 56 is formed of polysilicon single layer,

a silicide layer 62 is also formed on a top surface of the gate pattern 56. A silicide layer 62 is not formed around the dent D, such that a leakage current due to the structure of silicide layer 62 can be prevented.

Figs. 6 through 9 are cross-sectional views showing a method for fabricating a semiconductor device according to the second exemplary embodiment of the present invention.

Referring to Fig. 6, an isolation layer 52 is formed on a semiconductor substrate 50 to define an active region 54. A gate pattern 56 is formed on the active region 54. The isolation layer 52 is formed by a shallow trench isolation technique. In this case, there can be formed a dent D in the isolation layer neighboring the active region 54. A buffer oxide layer 70 is formed by applying a thermal oxidation process to the semiconductor substrate 50 to form a buffer oxide layer 70.

Referring to Fig. 7, a silicon nitride layer 72 and a silicon oxide layer 74 are sequentially formed on an entire surface of the semiconductor substrate 50 with the buffer oxide layer 70. At least one of the silicon nitride layer 72 and the silicon oxide layer 74 becomes thicker from the gate pattern 56 to the isolation layer 52. That is, at least one of the silicon nitride layer 72 and the silicon oxide layer 74 may be formed at an ambient of chamber having low temperature and low pressure. For instance, the silicon nitride layer 72 or the silicon oxide layer 74 may be formed of LTO or LTN made by LPCVD method with low temperature.

Referring to Fig. 8, the silicon oxide layer 74 is etched by an anisotropic plasma etching method to form outer spacers 74s having curved sidewalls. The silicon nitride layer 72 is etched using the outer spacers 74s

as an etch mask to form inner spacers 72s having L-shape cross-section interposed between the outer spacer 74s and the gate pattern 56. In this case, the active region 54 neighboring the lower edges of the gate pattern 56 is exposed first since one of the silicon nitride layer 72 and the silicon oxide layer 74 grows thicker from the gate pattern 56.

As illustrated in Fig. 9A, all the silicon nitride 72 and the silicon oxide layer 74 may be formed to grow thicker from the gate pattern 56 and the isolation layer 52.

Referring to Fig. 10A, the silicon oxide layer 74 is isotropically etched to form outer spacers 74s having curved sidewalls. The silicon nitride layer 72 is etched using the outer spacers 74s as an etch mask to form inner spacers 72s having L-shape cross-section interposed between the outer spacer 74s and the gate pattern 56. In this case, at least one of the silicon oxide layer 74 or the silicon nitride layer 72 may be etched using a plasma etching method under the condition of high bias power.

Alternatively, as illustrated in Fig. 9B, the silicon nitride layer 72 is formed conformally. The silicon oxide layer 74 may be formed to become thicker from the gate pattern 56 to the isolation layer 52.

Referring to Fig. 10B, the silicon oxide layer 74 is anisotropically etched to form outer spacers 74s and to form a blocking oxide layer 74a. Further more, using the outer spacers 74s and the blocking oxide layer 74a as an etch mask, the silicon nitride layer 72 is anisotropically etched to form inter spacers having L-shaped cross-section and a blocking nitride layer under the blocking oxide layer 74a. In this case, the silicon nitride layer 72 on the dent D is protected by the blocking oxide layer 74a, such

that the silicon nitride layer 72 may be etched using a conventional anisotropic etching method.

Referring to Fig. 11, after removing the buffer oxide layer 70, a silicidation process is applied to the semiconductor substrate to form a silicide layer 76 on the active region 54 exposed between the blocking insulation layer 74a and the spacers 74s and 72s. The silicide layer 76 may be formed on a top surface of the gate pattern 56.

The outer spacer 74s may be removed before the silicidation process, such that only L-shaped sidewall spacers 72s formed on both sidewalls of the gate pattern 56.

[Effect of the Invention]

According to the present invention, semiconductor devices with salicide source/drain except for around a dent of isolation layer can be fabricated. Therefore, it can be prevented that a leakage current flows due to a structure of silicide layer.

[Scope of Claim]

[Claim 1]

A semiconductor device, comprising:

an isolation layer formed in a semiconductor substrate to define an active region;

a gate patterned formed in the active region;

source/drain regions formed in the active region at both sides of the gate pattern;

sidewall spacers formed on sidewalls of the gate pattern;

a blocking insulation layer formed on the isolation layer and on a portion of the active region neighboring the isolation layer; and

a silicide layer formed on the source/drain regions between the blocking insulation layer and the sidewall spacers and having a boundary aligned to edges of the blocking insulation layer and the sidewall spacer.

[Claim 2]

The method of Claim 1, wherein the sidewall spacer comprises:

an inner spacer having L-shaped cross-section formed on the sidewall of the gate pattern and on the active region neighboring the gate pattern; and

an outer spacer having curved sidewall formed on the inner space.

[Claim 3]

The method of Claim 1, wherein the isolation layer includes a dent at the region neighboring the active region, and

wherein the blocking insulation layer is formed on the dent.

[Claim 4]

The device of Claim 1, further comprising a silicide layer formed on a top surface the gate pattern.

[Claim 5]

A method of fabricating semiconductor devices comprising:

forming a isolation layer in a semiconductor substrate to define an active region;

forming a gate pattern on the active region;

implanting impurities into the active region at both sides of the gate pattern;

forming a spacer insulation layer on an entire surface of the semiconductor substrate with the gate pattern, having a region becoming thinner from the isolation layer to the gate pattern;

anisotropically etching the spacer insulation layer to form sidewall spacers on sidewalls of the gate pattern, and to leave a blocking insulation layer on the isolation layer and on a portion of the active region neighboring the isolation layer; and

applying a silicidation process to the semiconductor substrate to form a silicide layer having a boundary aligned to the edges of the blocking insulation layer and the sidewall spacer on the source/drain regions

between the blocking insulation layer and the sidewall spacers.

[Claim 6]

The method of Claim 5, wherein the spacer insulation layer is formed by stacking a silicon nitride layer and a silicon oxide layer,

wherein at least one of the silicon nitride layer and the silicon oxide layer has a region becoming thinner from the field insulation layer to the gate pattern.

[Claim 7]

The method of Claim 6, wherein the forming the sidewall spacer comprises:

anisotropically etching the silicon oxide layer to form outer spacers having curved sidewall at both sides of the gate electrode; and

etching the silicon nitride layer using the outer spacers as an etch stop layer to form inner spacers having L-shaped cross-section between the outer spacers and the gate pattern.

[Claim 8]

The method of Claim 5, wherein the forming the spacer insulation layer comprises:

conformally forming a silicon nitride layer on the semiconductor substrate; and

forming a silicon oxide layer on the silicon nitride layer, having a region becoming thinner from the isolation layer to the gate pattern, and

wherein the forming the sidewall spacers and the blocking insulation layer comprises:

anisotropically etching the silicon oxide layer to form outer spacers on sidewalls of the gate pattern and to form a blocking oxide layer on the isolation layer and on a portion of the active region neighboring the isolation layer; and

etching the silicon nitride layer using the outer spacers and the blocking oxide layer as an etch mask to form inner spacers interposed between the outer spacers and the gate pattern and to form a blocking nitride layer interposed under the oxide spacers.

[Claim 9]

The method of Claim 5, wherein the forming the spacer insulation layer comprises:

forming a silicon nitride layer on the semiconductor substrate, having a region becoming thinner from the isolation layer to the gate pattern; and

conformally forming a silicon oxide layer on the silicon nitride layer, and

wherein the forming the sidewall spacers and the blocking insulation layer comprises:

anisotropically etching the silicon oxide layer to form outer spacers on the sidewalls of the gate pattern; and

etching the silicon nitride layer using the outer spacers as an etch mask to form a blocking nitride layer on the isolation layer and on a portion

of active region neighboring the isolation layer.

[Claim 10]

The method of Claim 5, wherein in the forming the sidewall spacers, the spacer insulation layer on the active region neighboring the gate pattern is etched at a rate faster than the etch rate of the spacer insulation layer on the active region neighboring the field insulation layer.